IN THE SPECIFICATION

Please amend the specification as follows:

In paragraph 0004 beginning on page 1 and ending on page 2, please amend the paragraph as follows:

-- **[0004]** As shown in FIG. 1, multi-bridge architectures can be viewed as having several different levels. A level 0 containing buses 122 and 124~~120~~ and devices 112A-112F, which may be collectively referenced as 112~~110~~, a level 1 containing bus-bridges 139~~130~~ and a level 2 including bridge-bridges 149~~140~~. Level 0 includes I/O devices 112~~110~~ connected to buses 122 and 124~~120~~. At level 1, bus-bridge~~bus-bridges~~ 139~~130~~ is~~are~~ connected to the buses 122 and 124~~120~~ of level 0. Further, the bus-bridge~~bus-bridges~~ 139~~130~~ has~~have~~ a transaction order queues (TOQ) 131~~135~~ and transaction buffers 186~~187~~ for each bus-bridge/bus link, such as bus-bridge/bus link 162~~160~~. TOQ 131~~135~~ stores transaction buffer identifiers for certain transactions to ensure that system ordering rules, such as PCI and PCI-X ordering rules, are not violated. The purpose of the TOQ 131~~135~~ is to ensure that transactions will execute in an order consistent with the system ordering rules. As such, not all transactions go into the TOQ, only those for which ordering rules apply. In contrast, transaction buffers store transaction information, such as cycle address, command, data, and the like. Next, level 2 contains one or more bridge-bridges, which may be represented by bridge-bridge 149~~140~~. ~~Each~~ Bridge-bridge ~~bridge-bridge~~ 149~~140~~ is connected to one or more bus-bridges, such as bus-bridge 139~~130~~ from level 1. Each bridge-bridge/bus-bridge link, such as bridge-bridge/bus-bridge link 152~~150~~ between bridge-bridge 149~~140~~ and bus-bridge 152,~~150~~ has one representative TOQ, which is TOQ 142,~~145~~ and one transaction buffer, such as transactional buffer 180,~~185~~ in the corresponding bridge-bridge 149~~140~~. An inherent difference between bus-bridge~~bus-bridges~~ 139~~130~~ and bridge-bridge~~bridge-bridges~~ 149~~140~~ is that bus-bridge~~bus-bridges~~ 139~~130~~ connect a series of buses 122 and 124~~120~~, while bridge-bridge~~bridge-bridges~~ 149~~140~~ connect a series of bridges. The bus-bridge's~~bus-bridges'~~ 139~~130~~ direct link to buses 122 and 124~~120~~ assures that bus-bridge~~bus-bridges~~ 139~~130~~ always know from which one of the buses 122 and 124~~120~~ a transaction originated. Bridge-bridge~~Bridge-bridges~~ 149~~140~~, in contrast, does~~do~~ not have a separate link for each of the buses 122 and 124~~120~~, and as such, are not inherently able to identify the bus source of any transaction. This inability to identify the bus source negatively impacts the ability for ordering transactions at the bridge-bridge

level, and as such, also unnecessarily limits the corresponding transactional throughput of the entire system. --

In paragraph 0005 beginning on page 2 and ending on page 3, please amend the paragraph as follows:

-- **[0005]** Transaction ordering, as discussed in more detail in the two U.S. patent applications incorporated below: U.S. Patent Application No. 09/749,111 by Paras Shah, ~~bearing Attorney Docket No. COMP:0189,~~ entitled "Relaxed Read Completion Ordering in a System Using a Transaction Order Queue," filed December 26, 2000, and issued into U.S. Patent No. 6,615,295 on September 2, 2003, and U.S. Patent Application No. 09/779,424, ~~bearing Attorney Docket No. COMP:0187,~~ entitled "Enhancement to Transaction Order Queue," filed February 8, 2001, orders a set of transactions based on a predefined set of rules. These rules are designed to achieve optimum transaction ordering where a single TOQ receives transactions originating from a single bus. However, where a TOQ receives transactions originating from multiple buses, optimum transaction ordering is lost and the overall transaction throughput is reduced. In further detail, and as shown in FIG. 1, TOQs 142~~145~~ and 131~~135~~, are used in two different types of bridges in two different levels. The first bridge, in level 2, is a bridge-bridge 149~~140~~, where single TOQs 142~~145~~ are used per each bridge-bridge/bus-bridge link (child-link) 152~~150~~, regardless of the number of buses 122 and 124~~120~~ attached to the corresponding bus-bridge 139~~130~~. The second bridge, at level 1, is a bus-bridge 139~~130~~, where single TOQs 131~~135~~ are used for each bus-bridge/bus link (grandchild-link) 160. In the case of a bus-bridge 139~~130~~, where there exists a one-to-one ratio between TOQs 131 and 132~~135~~ and buses 122 and 124~~120~~, a TOQ 131~~135~~, as designed, is limited to ordering the transactions from a single bus, and as such, is able to perform at its top design efficiency. However, in the case of a bridge-bridge 149~~140~~, where there exists a one-to-many ratio between TOQs 142~~145~~ to buses 122 and 124~~120~~, a TOQ 142~~140~~ is required to process transactions from multiple busses 122 and 124~~120~~ over a single child-link 152~~150~~. Specifically, TOQ 142 for example, is required to process transactions from multiple buses 122 and 124, and treat every transaction received through child-link 152, whether from bus 122 or bus 124, as though it originated from a single bus, and as such, the TOQ 142 is unable to function at its intended efficiency. In other words, because the bridge-bridge 149~~140~~ is unable to discern between transactions of different buses 122 and 124~~120~~ connected to a bus-bridge 139~~130~~, the bridge-bridge 149~~140~~ must order such transactions as

though they occurred on the same bus, bus 122 for example. Because of this, unnecessary blocking occurs where a blocking condition on one bus, bus 122 for example, is imposed, across the entire child-link, child-link 152 for example, effecting every attached bus 122 and 124~~120~~, and unnecessarily reduces transaction throughput. --

In paragraph 0011 on page 5, please amend the paragraph as follows:

-- **[0011]** U.S. Patent Application Serial No. 09/749,111, entitled "Relaxed Read Completion Ordering in a System Using a Transaction Order Queue," filed December 26, 2000 and issued as U.S. Patent No. 6,615,295 on September 2, 2003; and U.S. Patent Application Serial No. 09/779,424, entitled "Enhancement to Transaction Order Queue," filed February 8, 2001. --

In paragraph 0013 on page 5, please amend the paragraph as follows:

-- **[0013]** Level 0 represents a common architecture present in modern computer systems, (see FIG. 1 and buses 122 and 124~~120~~ and devices 112~~110~~), where multiple buses 280 are coupled with multiple I/O devices 290. Next, level 1, also a common architecture present in modern computer systems, (see FIG. 1 bus-bridge 139~~130~~), contains multiple bus-bridges 260 connected via grandchild-links 295 to multiple buses 280 where each such grandchild-link 295 has its own TOQs 270 for ordering the transactions for each individual bus 280. Also, each child-bridge 260 has one transaction buffer, i.e. 352, for each grandchild link, i.e., 296. Level 1's architecture, which provides a TOQ 270 for each connected bus 280, allows transaction ordering to occur in its most efficient form, i.e., one TOQ per one bus. --

In paragraph 0015 on page 6, please amend the paragraph as follows:

-- **[0015]** In further detail, level 2's TOQs are broken into as many sets 320 as there are child-links 285. Four child-links 286, 287, 288 and 289 in parent-bridge 232 are shown, and each link has an associated TOQ set 320: 321, 322, 323 and 324 respectively, as well as their own transaction buffers 349. Each of these respective child-links 286, 287, 288 and 289 includes multiple channels, such as channels 225A-225N, 226A-226N, 227A-227N, and 228A-228N. Further, within each TOQ set 320 are as many TOQs as there are grand-child links 295 for the associated child-link 285. For example, TOQ set 321, associated with child-link 286, and where such child-link 286 has four grand child links associated thereto: 296, 297, 298 and 299, is made up of four TOQs: 241, 242, 243 and 244. It should be noted that

TOQ 243 is drawn in phantom form to show that it could represent multiple TOQs to assure that there were an equal amount of TOQs in set 321 as grand-child links associated with child-link 286. Each of the TOQ sets 320 contains a phantom TOQ for the same purpose. The remaining TOQ sets disclosed are as follows: TOQ set 322 contains TOQs 245, 246, 247 and 248; TOQ set 323, representing none or more TOQ sets 320, contains TOQs 249, 250, 251 and 252; and TOQ set 324 contains TOQs 253, 254, 255 and 256. Each of these TOQs 241-256 may include a TOQ identifier, such as TOQ identifiers 441-456, which are discussed below in greater detail. Other embodiments may use less than one TOQ per grand-child link 295 for the associated child-link 285, but a minimum of two such TOQs are needed to optimize transaction ordering. Further, other multi-TOQ architectures may use more or less number of links to more or less number of child bridges. --

In paragraph 0016 beginning on page 6 and ending on page 7, please amend the paragraph as follows:

-- **[0016]** As discussed above, each of the TOQs 240 in parent-bridge 232 correspond with a grandchild-link 295. As such, each TOQ 240 is matched with a grandchild-link 295. A matching can be achieved in variety of ways. A matching can occur where the child-bridge transmits or originates a transaction identifier that is a predefined address of an associated TOQ 240. For example, in the case of TOQ set 321 having four TOQs 241, 242, 243 and 244, TOQ could have corresponding addresses 00, 01, 10 and 11. Thus, at the same time that child-bridge 260 is transmitting a transaction over child-link 286, the child-link 286 could transmit address 01 on a transaction identifier communication link, (two unused channels, such as channels 225A and 225B, on child-link 286 for example), such that parent-bridge 232 routes the transmission to TOQ 242. It is also contemplated that rather than identifying a TOQ by an address, it may be identified with a stored key or transaction order queue identifier, such as the keys or TOQ identifiers 441-456. Here, using the same transaction identifier 01, if each TOQ 240 had associated with it a key, the parent-bridge 232 could compare an incoming transaction identifier with each of the keys of each TOQ, and where there was a match, the parent-bridge would route the corresponding transmission to that TOQ, in this example again, TOQ 242. It is also contemplated that where a transaction is transmitted with a transaction identifier that does not match a key in any one of the TOQs 240, that the parent-bridge would route the transaction to a default TOQ, for example, TOQ 241. This assures that all transactions are handled. --

In paragraph 0017 on page 7, please amend the paragraph as follows:

-- **[0017]** In theory, the number of TOQs one could place within bridge-bridge 232 is limitless. However, in reality the number of TOQs employed in bridge-bridge 232 is limited by chip hardware constrains, such as size and complexity, and/or the ability and efficiency of uniquely identifying a transaction from a particular bus. In the disclosed embodiment, it is contemplated that a transaction is identified through a simultaneous transmission of an identifier from associated bus-bridge 260 to bridge-bridge 232 through an unused channel, such as one of the channels 225A-225N, on the child-links 285. In the case of a bus-bridge 260 having two buses attached via grandchild-links 295, bus 281 and bus 282, for example, a single channel could be used to transmit an identifier of either a "0" or a "1" to indicate which bus was the source of the transaction. However, where more than two buses 280 are attached to the bus-bridge 260, and a constraint exists which requires the use of only one channel, or for which only two TOQs are available, it is contemplated that the same single channel could still be used to handle the transactions by assigning buses 280, or grand-child links 295, an identifier of either "1" or "0," where the separate TOQs would handle buses of common identities as though they originated from a single source. As the number of buses rises, or the number of available TOQs increase, the need for additional channels arise. For example, where 4 buses and 4 TOQs are present, two channels (i.e., base 10's "3" = base 2's "11") would be needed, if however 8 buses and 8 TOQs are present, three channels (i.e., base 10's "7" = base 2's "111") would be needed. It should be noted that other means of identifying a transaction may occur through signals sent through dedicated connections between the bus-bridge 260 and the bridge-bridge 232, or means other than an unused channel in child-links 285. --

In paragraph 0018 on page 8, please amend the paragraph as follows:

-- **[0018]** It is contemplated that if the disclosed embodiment is implemented with a typical parent-bridge 140 as found in FIG. 1, i.e., a parent-bridge with only one TOQ per child-links 285, rather than a parent-bridge 232 which has multiple TOQs per child-links 285, that this implementation would result in a system with the same throughput as the typical architecture shown in FIG. 1. This is because although a bus identification signal would be sent to the parent-bridge 232, there would be no functionality to receive it, nor any additional TOQs to take advantage of the information if it could be received, and thus, the parent-bridge 232 would simply order all the transactions coming through a particular child-link 285 as

though they were originating from the same bus 280, or grand-child link 295, i.e., the same result as what is occurring at parent-bridge 140 in FIG. 1. Further, it is also contemplated that if the disclosed embodiment, having at least one parent-bridge 232 that in turn has multiple TOQs 240 per its child-links 286, is implemented without a child-bridge 260 that either originates or transmits bus identification signals to the parent-bridges 232, i.e, the child-bridge 162~~160~~ of FIG. 1, that this implementation would also function with the same throughput as the architecture of FIG. 1. This is because the parent-bridge 232 would receive each transaction without any bus identification signal and for parent-bridge 232 to receive a transaction without an identification signal is the same as if it received a transaction with an address of "0." Thus, all the transactions received by parent-bridge 232 would be directed to a single TOQ resulting in the same throughput experienced by the system of FIG. 1. --

In paragraph 0021 beginning on page 9 and ending on page 10, please amend the paragraph as follows:

-- **[0021]** In even greater detail, level 3's TOQs are broken into as many sets 310 as there are child-links to bridge-bridge 200. Specifically, four child-links 221, 222, 223 and 224 are shown in parent-bridge 200, and each link has an associated TOQ set 310: 311, 312, 313 and 314 respectively, as well as their own transaction buffers 339. The child link 221 may include channels 219A-219N, which may any number of channels that are utilized to communicate with the parent-bridge 232. It should also be appreciated that each of the other child-links may include various channels, as well. Further, within each TOQ set 310 there are as many TOQs 218 as there are grand-child links 285 for the associated child-link 220. For example, TOQ set 311, associated with child-link 221, and where such child-link 221 has four grand child links associated thereto: 286, 287, 288 and 289, is made up of four TOQs: 201, 202, 203 and 204. It should be noted that TOQ 203 is drawn in phantom form to show that it could represent multiple TOQs to assure that there were an equal amount of TOQs in set 311 as grand-child links associated with child-link 221. Each of the TOQ sets 310 contain a phantom TOQ for the same purpose. The remaining TOQ sets disclosed are as follows: TOQ set 312 contains TOQs 205, 206, 207 and 208; TOQ set 313 representing none or more TOQ sets 310, contains TOQs 209, 210, 211 and 212; and TOQ set 314 contains TOQs 213, 214, 215 and 216. Each of these TOQs 201-216 may include a TOQ identifier, such as TOQ identifiers 401-416, which are similar to the TOQ identifiers 441-456 discussed above. Other embodiments may use less than one TOQ per grand-child link 285 for the associated child-

link 220, but a minimum of two such TOQs are needed to optimize transaction ordering. Further, other multi-TOQ architectures use more or less number of links to more or less number of child-bridges or grandchild-links. --